



CONSTRUCTION OF COSMIC RAY DETECTORS CRD/ANALYSIS OF THE FAN-OUT BOARD FOR THE QUARKNET PROJECT

Adenrele Fapohunda

Engineering Department

Electrical Engineering

Benedict College

1600 Harden St.

Columbia, SC 29204



Supervisor:

Thomas Jordan

Education Program Leader

Fermi National Accelerator Laboratory

Batavia, IL 60510-0500

August 10, 2006

TABLE OF CONTENTS

Abstract.....	4
Introduction	
What are cosmic rays?	4
Detection.....	5
Hardware Overview of CRD.....	7
Diagram of DAQ Board.....	8
Use of DAQ Board in a DAQ Board	9
The QuarkNet Fan-Out Board.....	10
Project Description	
Purpose and Use of QuarkNet Fan-Out Board (QFB).....	11
How the Board Works.....	11
Connection with Fan-Out Board.....	12
QFB Schematic Diagram.....	13
Technical Details/Board Components Functionality.....	14
Conclusion.....	14
Acknowledgements.....	14
References.....	15
Appendices	
Appendix A.....	16
THE DS90C031BTM.....	16
Features of the DS90C031BTM.....	16
Connection/Functional Diagrams.....	16
Pin Descriptions.....	18
Appendix B.....	19

THE DS90C402.....	19
Features of the DS90C402.....	20
Connection/Functional Diagram.....	20
Appendix C.....	21
RS 232.....	21
Voltage Levels.....	22
Interface Basics.....	23
RS 232 signal Levels.....	23,25

ABSTRACT:

This research paper focuses on the construction of Cosmic Ray Detectors (CRD) with a specific concentration on the Fan-Out Board. Working with the Education Office, under the QuarkNet program, I and a team of other interns were responsible for assembling seventy-five CRDs, which were sent to high schools, colleges and universities and were used to perform experiments. It should be noted that the construction of CRDs was a process carried out in the background whilst my research was specifically the analysis, replicating and troubleshooting of the Global Positioning System (GPS) fan-out board.

INTRODUCTION:

QuarkNet is a teacher professional development program funded by the National Science Foundation and the U.S. Department of Energy. Teachers work on particle physics experiments during a summer and join a group of scientists and teachers working to introduce some aspects of their research into their classrooms. As interns with QuarkNet this summer, we primarily had to construct and test components of the CRD. Primarily, the new design of the a CRD array was less cumbersome and less liable to breakage as were the old ones. In order to understand the idea behind the setup of the cosmic ray detector, it is essential that I shed light on the definition of cosmic rays and some other ambiguous terms.

WHAT ARE COSMIC RAYS?

Cosmic rays are radiation consisting of energetic particles originating beyond the Earth that strike the Earth's atmosphere. Cosmic rays are composed mainly of bare nuclei, roughly 87% protons, 12% alpha particles (the nuclei of helium atoms) and most of the rest being made up of heavier atomic nuclei with relative abundances comparable to those found in the Sun. Electrons, gamma rays, and very high-energy neutrinos also make up a much smaller fraction of the cosmic radiation.

DETECTION

The nuclei that make up cosmic rays are able to travel from their distant sources to the Earth because of the low density of matter in space. Nuclei interact strongly with other matter, so when the cosmic rays approach Earth they collide with the nuclei of atmospheric gases. These collisions, in a process known as a shower, result in the production of many pions and kaons, unstable mesons which quickly decay into muons. Because muons do not interact strongly with the atmosphere and because of the relativistic effect of time dilation, many of these muons are able to reach the surface of the Earth. Muons are ionizing radiation, and may easily be detected by many types of particle detectors such as bubble chambers or *scintillation detectors*. If several muons are observed by separated detectors at the same instant, it is clear that they must have been produced in the same shower event. The kinetic energies of cosmic ray particles span over fourteen orders of magnitude, with the flux of cosmic rays on the Earth's surface falling approximately as the inverse-cube of the energy. Cosmic rays originate from energetic processes on the Sun all the way to the farthest reaches of the visible universe. Cosmic rays can have energies up to 10^{20} eV [1].

The construction of CRD is divided into three phases:

- 1) Assembly
- 2) Testing
- 3) Packaging

ASSEMBLY:

This stage includes tasks such as:

Soldering stereo jacks onto the Photo Multiplier Tubes (PMT) and also crimping BNC connector onto them.

Gluing the cookies onto the scintillator and then completely wrapping them up in aluminum foil and Marvel Guard. The entire scintillator is eventually covered up with electrical tape to prevent the escape of light as well as the interference of ambient light.

Cutting of poly vinyl chloride (PVC) pipes,
Construction/assembly of components of power distribution boxes.

TESTING:

This stage includes:

Testing for shorts in the PMT.
Using the Oscilloscope and the pulse generator to confirm sanity of PMT.
Testing for the power distribution boxes.
Testing for continuity in the GPS cables.

PACKAGING:

This is the final stage where all components of the CRD are collated and shipped to the various locations.

Below is a complete setup of a CRD array complete to view cosmic showers

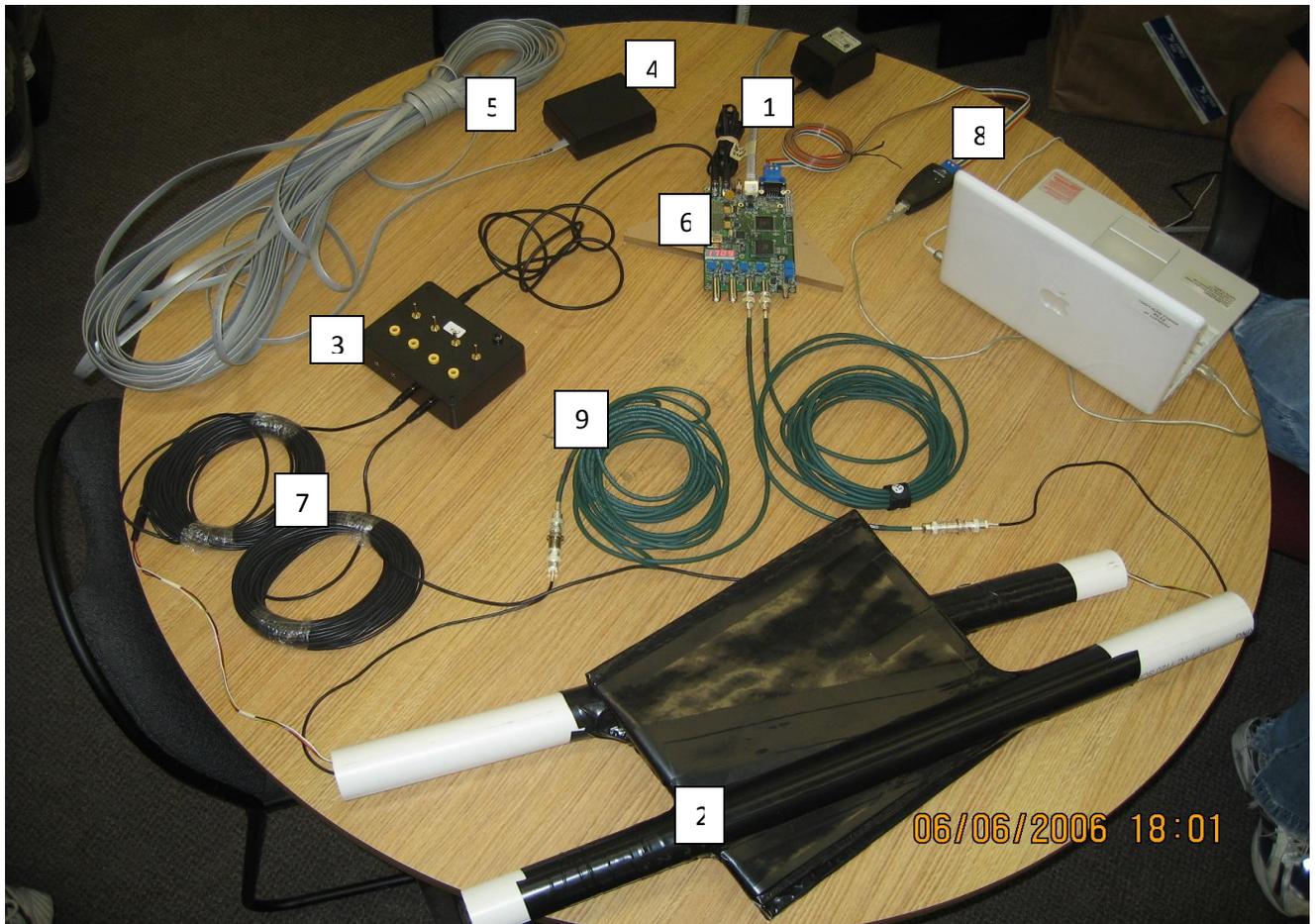


Figure 1. A typical CRD setup

HARDWARE OVERVIEW

1. 5 VDC adapter
2. Counters---scintillators, PMT
3. Power Distribution Boxes (PDB)
4. GPS receiver/antenna
5. GPS extension cable
6. Data Acquisition Board (DAQ) Board.
7. Power cable
8. Optional RS-232 to USB adapter (to link to computer USB port instead of serial port)
9. Signal cables

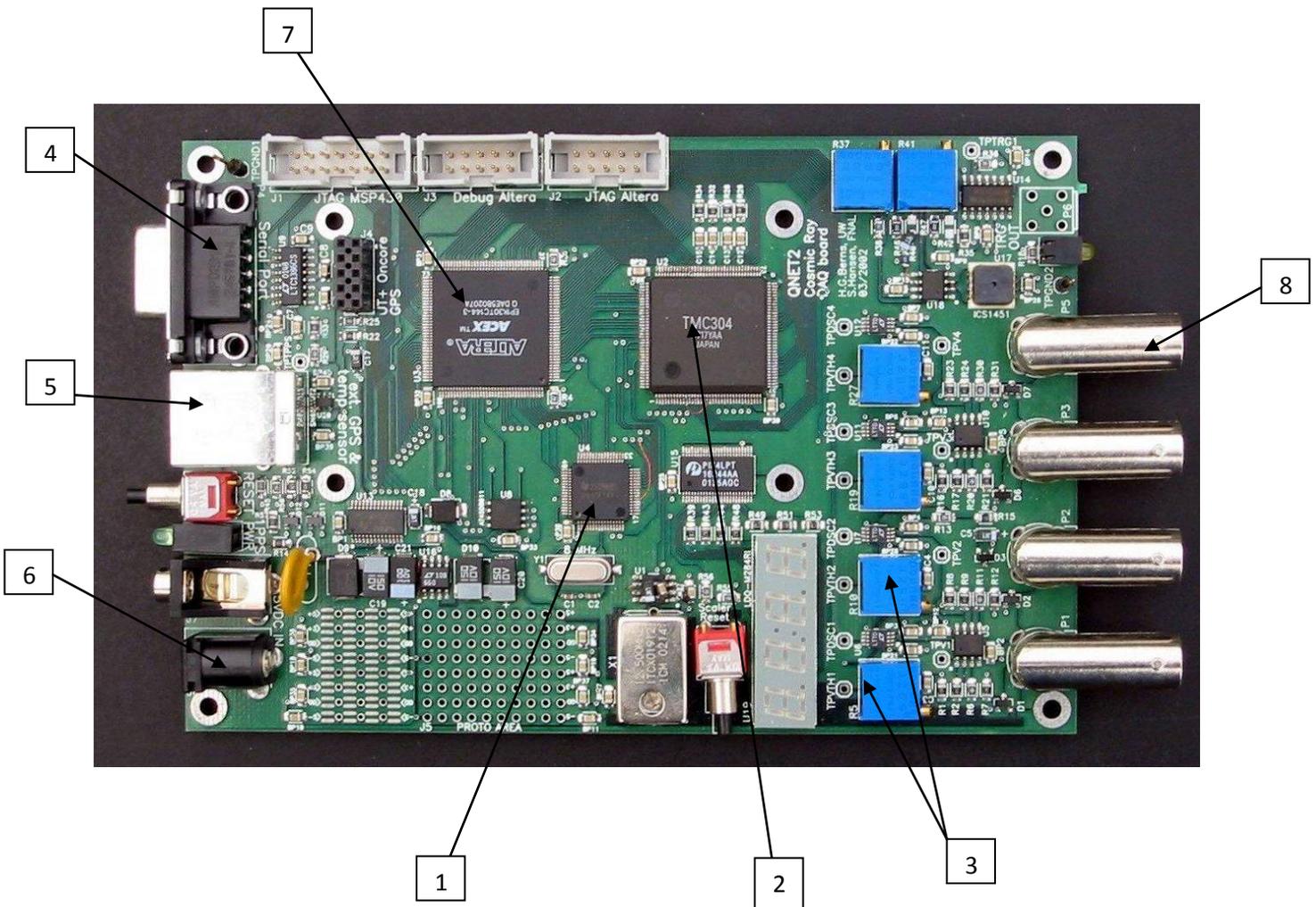


Figure 2 . The QuarkNet DAQ v2 board with major components labeled.

- 1) Microcontroller (programmable slow logic/interface)
- 2) Time-to-Digital Converter (TMC)
- 3) Discriminators
- 4) Serial port (output to PC)
- 5) GPS input
- 6) 5 VDC input
- 7) CPLD (programmable fast Logic)
- 8) One of 4 inputs for 4 counter signals (channels 0 through 3)

USE OF GPS IN THE DAQ BOARD

The GPS receiver automatically scans the sky for appropriate GPS satellite signals and by default switches to navigation mode. When the first satellite is tracked, the receiver initializes a one pulse per second (PPS) mode, which then triggers the CPLD counter on the board. The CPLD counter uses the precision PPS for logging the time of event triggers with 24-nanosecond accuracy; the timing is however not accurate until it tracks at least four satellites. The GPS reception status can be checked by typing the command DG (Display GPS status) on the Z-term software that runs the array. Once this status is verified, the 1PPS signal will usually stay accurate around absolute UTC with an estimated error of 50 nanoseconds rms or over and board operations can then commence [2]

The Leadtek GPS-9532W module is connected to the QuarkNet DAQ card through a cable, custom made for the board, with a male 10-pin RJ-45 connector at each end. The Leadtek module terminators into a custom circuit board with resistor-capacitor (RC) filters for the 5 VDC supply voltage for the GPS receiver and RS-232 serial signals and a Low Voltage Differential Signal (LVDS) driver for the 1 PPS pulse. This allows transmission over long unshielded cables having lengths up to 30 m without decaying. The circuit board also has a temperature sensor to allow monitoring the outdoor temperature at the GPS receiver.

The QuarkNet Fan-Out Board

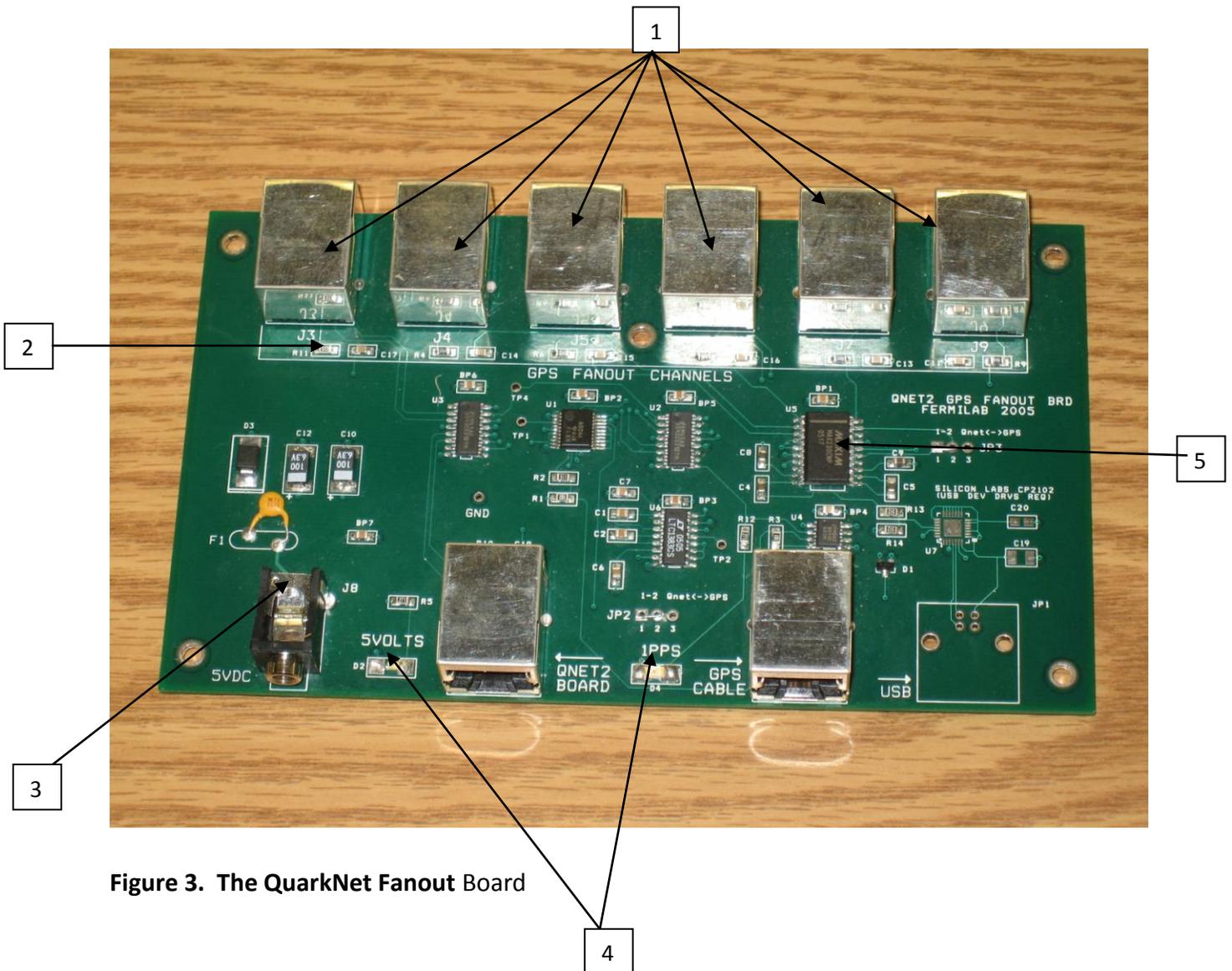


Figure 3. The QuarkNet Fanout Board

- 1) RJ-45 (6 GPS inputs)
- 2) Resistor
- 3) 5 VDC
- 4) Light Emitting Diode (LED)
- 5) IC (Max 230/SO)

PROJECT DESCRIPTION

I concentrated on the analysis of the QuarkNet fan-out board. In doing this, I had to replicate a model of the fan-out board. Page 13 shows a schematic diagram of the fan-out board which I worked on to produce a similar version of the prototype board.

PURPOSE/USE OF THE QUARKNET FANOUT BOARD

It would be observed from the set up array of CRD that the fan-out board was initially not a part of the experiment. Hence the question that comes to mind is as to the functionality and the reason behind the design, construction and inclusion of the fan-out board in the CRD array.

Before the invention of the Fan-out board in November 2005 by Terry Kiper and Constantin Fanaroukis, multiple DAQ boards at one location required individual GPS antennae--one dedicated to each board. This required much cabling and careful placement of antennae. This problem called for a solution to multiply or fanout the signal from 1 GPS to several DAQ boards.

HOW THE BOARD WORKS

Basically, the QuarkNet fan-out Board works using the principle of RS-232. RS-232 is a standard for serial binary data interconnection between a *DTE* (Data Terminal Equipment) and a *DCE* (Data Communication Equipment). The GPS cable that goes into the input RJ45 uses RS 232. The board however requires that the signal comes in as a logic such that the particular IC chip specified for this chip can process it and then fan-out the input into six different places. Hence, an RS 232 to a TTL (Transistor-Transistor-Logic) converter is required to transform the signal to a Logic recognized by the logic circuit. After this is accomplished, the chip successfully fans out the input produced six different ways, maintaining a required voltage. At the other end of the board, right before it reaches the other six RJ45s at the other end, the signal is converted from TTL back to RS232 and this summarizes the process used in fanning out one input six different ways. Further information is available on RS-232 and TTL in Appendix C.

Figure 4 below shows two DAQ connections to the QuarkNet fan-out board. Arrow number 1 points to J1. J1 is the RJ45 which connects to the outside antenna, which could be anywhere in

an open space – the QuarkNet’s major GPS antenna is situated on the roof of Wilson Hall. Arrow number 2 points to another RJ45, J2, which has a cable going from one point on the fan-out board to another DAQ board. This is the main DAQ board and it can send commands to and receive data from the antennae. Arrow number 3 points specifically to, but is not limited to, J3. J3 is another RJ45 that is connected from one point on the fan-out board to another DAQ board board via a GPS cable. Unlike the DAQ board connected to J2, these DAQ boards are slaves and all they can do is listen; they cannot transmit raw data as compared to J2 and they are hence referred to as slaves. Similarly, J4 through J9 perform the same task as J3 with each of them being connected to individual DAQ boards.

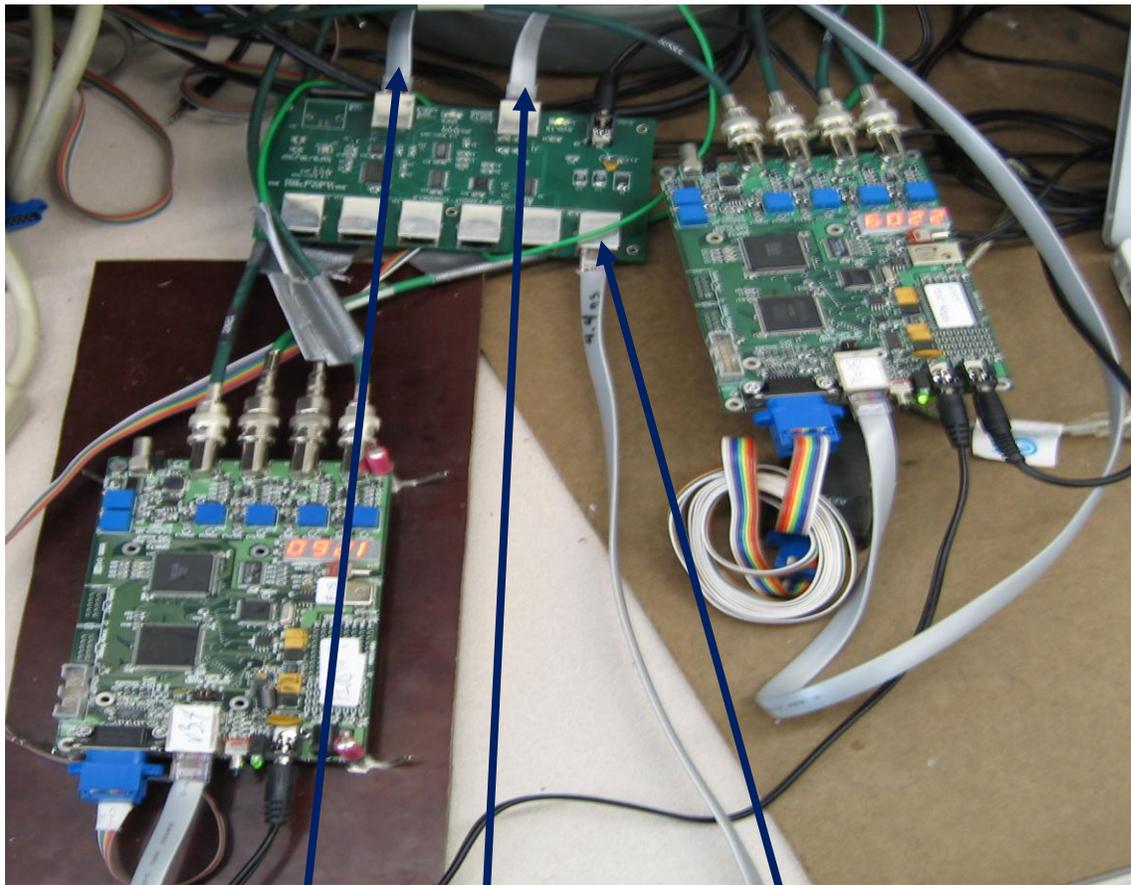
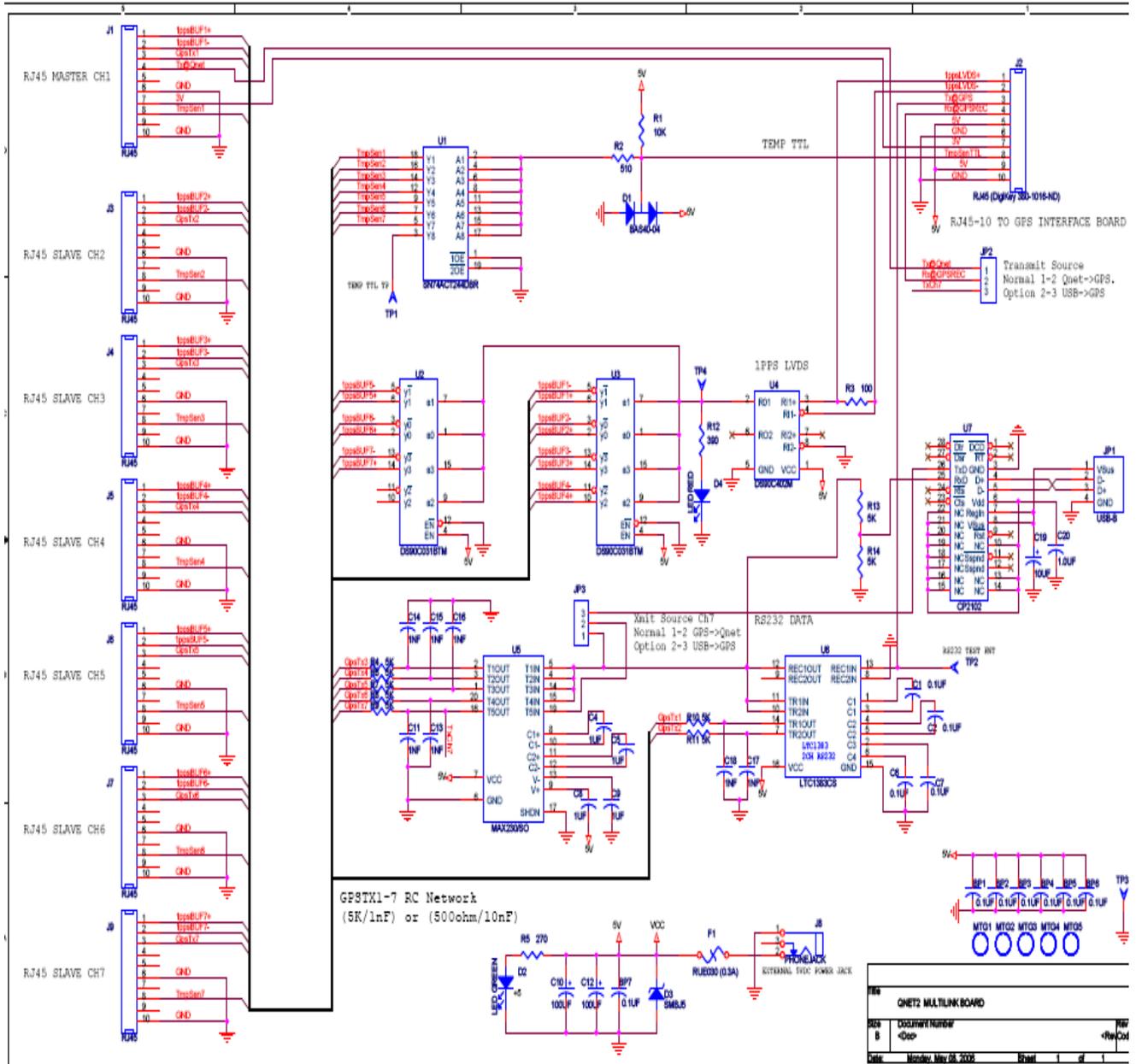


Figure 1: Connection with Fan-out Board

1

2

3



TECHNICAL DETAILS/BOARD-COMPONENTS FUNCTIONALITY

There are two major ICs present in the QuarkNet fan-out Board; they are **DS90C031BTM** and **DS90402**. Their significance and importance cannot be underestimated and at such, I have chosen to discuss the details of their functionality. The details of these components can be found in Appendices A and B.

CONCLUSION:

Under the supervision of my Supervisor, Thomas Jordan, I was able to assemble materials necessary to produce 75 cosmic ray detectors (CRDs) . Similarly I got a little more in depth knowledge into troubleshooting and assembling power distribution boxes (PDB), which took an input of 5V, and outputted a voltage ranging from 0.3 V to 1.8 V.

Most importantly, and more specifically, I got to replicate the QuarkNet fan-out board, troubleshoot it, and lent more about the theory behind the components of the board that puts it to perform the kind of work it does In the entire setup of the CRD.

ACKNOWLEDGEMENTS

I would first and foremost like to thank the Almighty God for giving me the opportunity to wield an intern position with the QuarkNet program at in Fermi National Accelerator Laboratory, a position I intend to come back to either as a fulltime workers with your permission of course-or as an intern in the nearest future. I would secondly like to thank the Dianne Engram, manager of Equal Opportunity Office, Elliot McCrory, chairman of the SIST Program, and the SIST Committee for deeming me fit to be a part of this ennobled program at Fermilab. I would also more importantly like to thank my supervisor, Thomas Jordan, for squeezing out time from his tight schedule to work with me as an intern this summer and helping me with areas that were very much alien to me from the start. I would also like to thank Bob Peterson, David Hoppert, Terry Kiper, and the rest of my summer colleagues. I thank each and every one of them for making my learning/internship experience a wonderful one. I could not have done it without of them all. Last but not the least, my thanks go out to all those hardworking physicists and

engineers, who I never got to see, but whose ongoing research and technological innovations made it possible for me to be here and make it possible for Fermilab to be what it is. It has been great and I look forward to coming back and doing some more engineering-related work.

Thanks again.

REFERENCES

[1] NASA's Goddard Flight Center, (2006, May), *Introduction to Cosmic rays*

http://imagine.gsfc.nasa.gov/docs/science/known/cosmic_rays.html

[2] Hans-Gerd, Toby H. Burnett, Richard Gran and R. Jeffery Wilkes, "GPS Time Synchronization in School-Network Cosmic Ray Detectors," *IEEE Trans. Nuclear Science*, vol. 51, no 3, pp. 850, 2004.

[3] Digi-key Corporation, (2003, September), *Technical/Catalogue information on DS90C032B*

<http://rocky.digikey.com/scripts/ProductInfo.dll?Site=US&V=14&M=DS90C032BTM>

[4] National Semiconductor, (2005 August), *Technical/Catalogue information on DS90C402*

<http://www.national.com/ds/DS/DS90C402.pdf>

[5] Pinouts.ru team, (2005, March), RS-232 (EIA-232) serial interface pinout

http://pinouts.ru/SerialPorts/RS232_pinout.shtml

[6] Adrio Communications Ltd. An overview of RS232 Communication Standard

http://www.radio-electronics.com/info/telecommunications_networks/networking/rs232/rs232.php

APPENDIX A

THE DS90C031BTM – LOW VOLTAGE DIFFERENTIAL SIGNAL (LVDS)

This is a quad CMOS (Complementary-symmetry/metal-oxide semiconductor (CMOS), is a major class of integrated circuits. CMOS chips include microprocessor, microcontroller, static RAM, and other digital logic circuits) differential line driver designed for applications requiring ultra low power dissipation and high data rates. It is designed to support data rates in excess of 155.5Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C031B accepts TTL/CMOS (TTL stands for **Transistor-Transistor Logic**) It is a class of digital circuits built from bipolar junction transistors (BJT), and resistors. It is notable for being a widespread integrated circuit (IC) family used in many applications such as computers, industrial controls, music synthesizers, and electronic test and measurement instruments) input levels and translates them to low voltage (350 mV) differential output signals. In addition, the driver supports a TRI-STATE function that may be used to disable the output state, disabling the load current and thus dropping the device to an ultra low idle power state of 11 mw typical. This IC also provides a power-off high impedance LVDS outputs. This feature assures minimal loading effect on the LVDS bus lines when Vcc is not present. The DS90C031B and companion line receiver (DS90C032B) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications. [3]

FEATURES OF THE DS90C032B

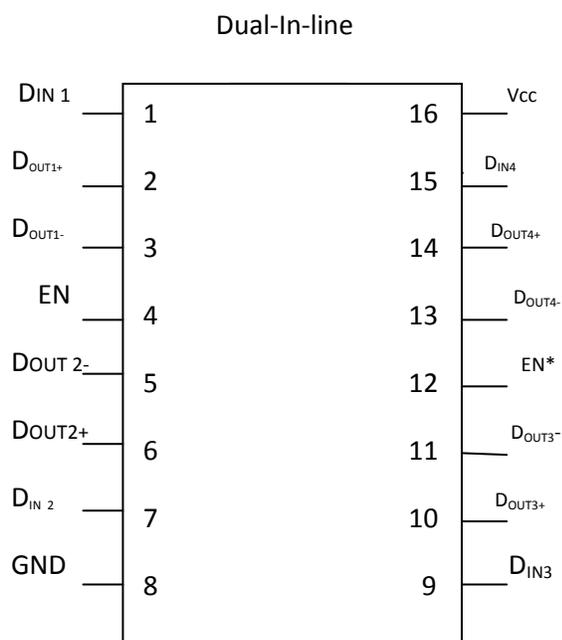
- 15.5 Mbps (77.7 MHz) switching rates
- High Impedance LVDS outputs with power-off
- +/-350mv differential signaling
- Ultra low power dissipation
- Fail-safe logic for floating inputs
- 400 ps maximum differential skew (5V, 25°C)

3.5 ns maximum propagation delay

Industrial operating temperature range

Conforms to ANSI/TIA/EIA-644 LVDS standard. [3]

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

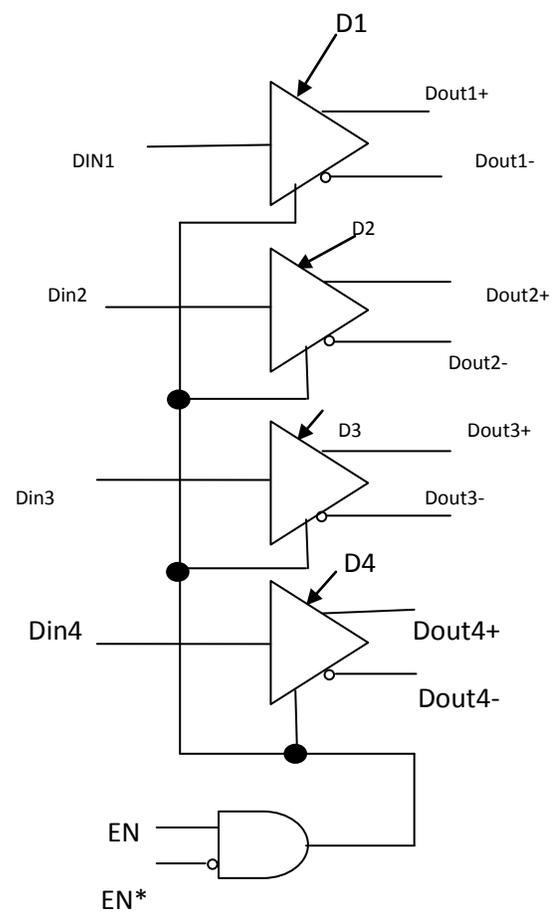


FIG 5. DS90C032B Functional and connection Diagram

PIN DESCRIPTIONS

Pin number 1 7 9 and 5 (Din) are the driver input pin and are TTL/CMOS compatible. Pins 2, 6, 10 and 14 (Dout+) are the non-inverting output pins. They are at LVDS levels. Pins 3, 5, 11 and 13 (Dout-) are inverting driver output pin and are also at LVDS level. Pin 4 is an active high enable pin, OR-ed with EN*. 12 is an active low enable pin, OR-ed with EN. Pin 16 is the power supply pin, +/-5 V +/- 10%. Pin 8, is the ground pin. [3]

APPENDIX B

THE DS90C402 – DUAL LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) Receiver

The DS90C402 is a dual receiver device optimized for high data rate and low power applications. This device along with the DS90C401 provides a pair chip solution for a dual high-speed point-to-point interface. The device is a PCB space saving 8-lead small outline package. The receiver offers +/-100 mv threshold sensitivity, in addition to common-mode noise protection. [4]

FEATURES OF THE DS90C402

Ultra Low-Power Dissipation

Operate above 155.5 Mbps

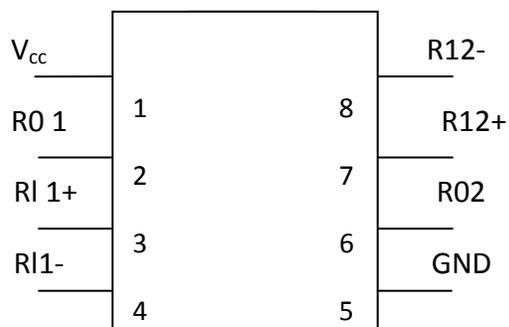
Standard TIA/EIA-644

8 lead SOIC Package saves PCB space

+/- 100 mV Receiver Sensitivity

Vcm +/-1 V center around 1.2 V [4]

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

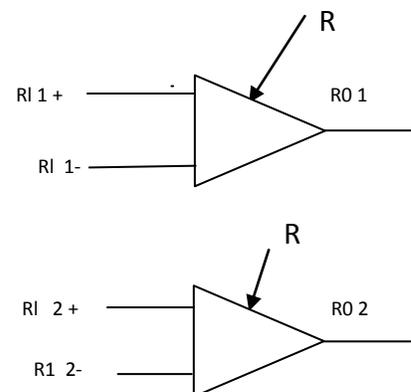


Figure 6. DS90C402 functional and connection diagrams

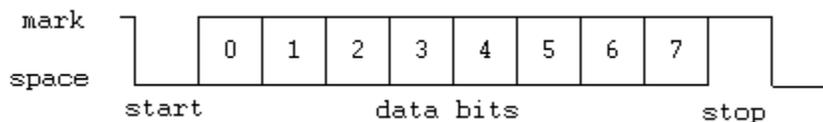
LVDS drivers and receivers are intended primarily to be used in an uncomplicated point-to-point configuration. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω . A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. [4]

APPENDIX C

RS-232

RS-232 is a standard for serial binary data interconnection between a *DTE* (Data Terminal Equipment) and a *DCE* (Data Communication Equipment). It is commonly used in computer serial ports. A similar ITU-T standard is **V.24**. **RS** is an abbreviation for "Recommended Standard."

In RS-232, data is sent as a time-series of bits. Both synchronous and asynchronous transmissions are supported by the standard. Each circuit only operates in one direction, that is, signaling from a DTE to the attached DCE or the reverse. Since transmit data and receive data are separate circuits, the interface can operate in a full duplex manner, supporting concurrent data flow in both directions. The standard does not define character framing within the data stream, or character encoding.



The most common arrangement, nearly universal in personal computers, is an asynchronous link sending seven or eight bits. When used in this way, the bit order consists of a start bit, seven or eight data bits sent least significant bit first, an optional parity bit, and a stop bit. The steady state of the line is called the Marking state. The start of a new character is signaled by a change to the Space state. The digital ones and zeros are then transmitted serially onto the line by switching between the Mark and Space state ending with a final stop bit which is a transition back to the Marking state. [6]

VOLTAGE LEVELS

The RS-232 standard defines the voltage levels that correspond to logical one and logical zero levels. Signals are plus or minus 3 to 15 volts. The range near zero volts is not a valid RS-232 level; logic one is defined as a negative voltage, the signal condition is called marking, and has the functional significance of OFF. Logic zero is positive, the signal condition is spacing, and has the function ON. The standard specifies a maximum open-circuit voltage of 25 volts; signal levels of ± 5 V, ± 10 V, ± 12 V, and ± 15 V are all commonly seen depending on the power supplies available within a device. Circuits driving an RS-232-compatible interface must be able to withstand indefinite short circuit to ground or to any voltage level up to 25 volts. The slew rate, or how fast the signal changes between levels, is also controlled.

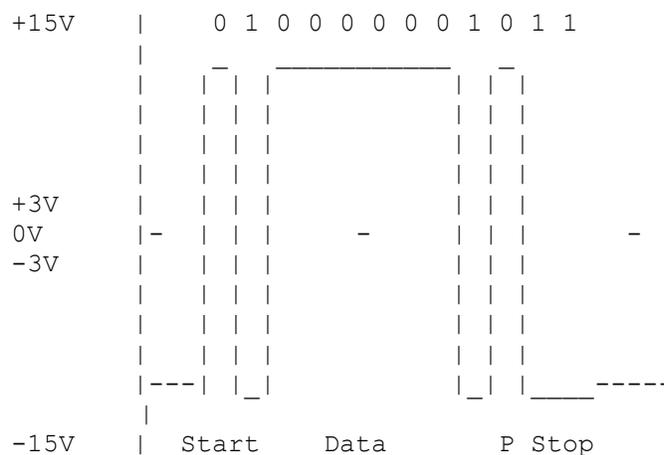


Figure 7: RS-232 Flow diagram [5]

INTERFACE BASICS

The interface is intended to operate over distances of up to 15 meters. This is because any modem is likely to be near the terminal. Data rates are also limited. The maximum for RS-232C is 19.2 k baud or bits per second although slower rates are often used. In theory it is possible to use any baud rate, but there are a number of standard transmission speeds used.

Common Data Transmission Rates are 50, 75, 110, 150, 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 76800

Note: Speeds up to 19200 bits per second are normally used. Above this noise that is picked up, especially over long cable runs can introduce data errors.

RS-232 SIGNAL LEVELS

The voltage levels are one of the main items in the specification. For RS232 data signals a voltage of between -3 V and -25 V represents a logic 1. The logic 0 is represented by a voltage of between +3V and +25V. Control signals are in the "ON" state if their voltage is between +3 V and +25 V and "OFF" if they are negative.

The data is sent serially on RS-232; each bit is sent one after the next because there is only one data line in each direction. This mode of data transmission also requires that the receiver knows when the actual data bits are arriving so that it can synchronize itself to the incoming data. To achieve this, a logic 0 is sent as a start bit for the synchronization. This is followed by the data itself and there are normally seven or eight bits. The receiver obviously has to know how many data bits to expect hence there are often small dual-in-line switches either on the back of the equipment or inside it to set this information.

Data on RS 232 is normally sent using ASCII (American Standard Code for Information Interchange). However, other codes including the Murray Code or EBCDIC (Extended Binary Coded Decimal Interchange Code) can be used equally well.

After the data itself, a parity bit is sent. Again, this requires setting because it is optional and it can be even or odd parity. This is used to check the correctness of the received data and it can indicate whether the data has an odd or even number of logic ones. Unlike many systems, these days there is no facility for error correction.

Finally a stop bit is sent. This is normally one bit long and is used to signify the end of a particular byte. Sometimes two stop bits are required and, again, this is an option that can often be set on the equipment.

RS-232 data transmission is normally asynchronous. However, transmit and receive speeds must obviously be the same. A certain degree of tolerance is allowed. Once the start bit is sent, the receiver will sample the center of each bit to see the level. Within each data word the synchronization must not differ by more than half a bit length; otherwise the incorrect data will be seen. [6]